Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.110”**

**ANODE**

**.098 x .098”**

**.013”**

**.110”**

**Top Material: Ti/Ni/Ag**

**Backside Material: Si**

**Bond Pad Size: .098”**

**Backside Potential: ANODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .110” X .110” DATE: 4/27/23**

**MFG: VISHAY THICKNESS .013” P/N: TV110B030A6NU**

**DG 10.1.2**

#### Rev B, 7/1